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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MASON, DONNA K	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/810,746	FALIK ET AL.	
	Examiner	Art Unit	
	Donna K. Mason	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days; a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6,50-60 and 70-73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6,50-60 and 70-73* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2-4, 50-54, and 70-73 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,339,443 to Lockwood.

With regard to claims 2, 50, and 53, Lockwood discloses a method and a system (*see generally*, Fig. 1, item 10) for allowing shared access by at least two processors (Fig. 1, items 12a-12n) including an embedded controller and a host processor (column 4, lines 18-31) to at least two modules, the system including: at least two modules (Fig. 1, item 16; column 4, lines 67-68 to column 5, lines 1-4); a transaction control (Fig. 1, item 18; column 4, lines 32-35), where the embedded controller is capable of providing an indication of which of the at least two modules to access to the transaction control (Fig. 1, item 14; column 4, lines 54-65); and where the host processor is capable of providing an indication of which of the at least two modules to access to the transaction control (Fig. 1, item 14; column 4, lines 54-65); and at least one access block bit controlled by one of the at least two processors for blocking access by another of the at least two processors to at least one of the at least two modules (column 5, lines 25-36). With further regard to claim 53, see generally column 4, lines 61-65, column 7, lines 16-24, and column 7, lines 43-59).

It should be noted that although the "access block bits" disclosed in Lockwood are described as "access grant bits", the grant bits of Lockwood perform the same function as the block bits, as claimed. That is to say, the disclosed grant bits "block access by another of the at least two processors to at least one of the at least two modules," as claimed (*see* column 4, lines 42-52).

With regard to claims 3, 51, 52, 72, and 73, Lockwood discloses a method and system, where the at least one access block bit is capable of enabling at least one of the at least two modules (column 5, lines 53-58); and where the indication from each of the at least two processors is for a different module to access (column 4, lines 54-68 to column 5, lines 1-11).

With regard to claims 4, 54, and 55, Lockwood discloses a method and system further including: a bus extension; where at least one of the at least two modules is accessible via said bus extension; where the transaction control is capable of providing to the bus extension an indication of the at least one of the modules, accessible via the bus extension, for access by the host processor; where the transaction control is capable of providing to the bus extension an indication of the at least one of the modules, accessible via the bus extension, for access by the embedded controller; and where the bus extension is capable of providing an indication of the at least one of the modules for access by one of the processors. (*See generally*, column 4, lines 32-53).

With regard to claims 70 and 71, Lockwood discloses the method and system where at least one of the at least two modules includes a memory accessible through the bus extension (column 4, lines 32-61).

Therefore, Lockwood reads on the invention as specified in claims 2-4, 50-54, and 70-73.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-6, 50-60, 72, and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,260,098 to Ku in view of U.S. Patent No. 5,214,778 to Glider, et al. ("Glider").

With regard to claim 2, Ku discloses a system (Fig. 5, item 600) for allowing shared access by at least two processors including an embedded controller (Fig. 5, item 620 and column 11, lines 19-21) and a host processor (Fig. 5, item 602) to at least two modules (Fig. 5, items 622 and 622b) including: at least two modules (Fig. 5, items 622 and 622b); and a transaction control (Fig. 5, item 100); where the embedded controller is capable of providing an indication of which of the at least two modules to access to said transaction control (column 5, lines 34-61); and the host processor is capable of providing an indication of which of the at least two modules to access to said transaction control (column 5, lines 2-33 and lines 54-61).

With regard to claim 50, Ku discloses a method for allowing shared access to at least two modules (Fig. 5, items 622 and 622b) by at least two processors including an embedded controller (Fig. 5, item 620 and column 11, lines 19-21) and a host processor (Fig. 5, item 602), including the steps of: receiving an indication from each of the at least two processors of a module from among the at least two modules to access (column 5, lines 9-53); arbitrating between the at least two processors in favor of one of the at least two processors (column 5, lines 2-8); and accessing said module indicated by said one of the at least two processors (column 5, lines 30-33 and column 6, lines 18-20).

With regard to dependent claims 3, 51, 52, 72, and 73 Ku discloses the method and system, the method further including the step of: blocking access by another of the at least two processors to said module indicated by said one of the at least two processors (column 4, lines 57-63), and where the indication from each of the at least two processors is for a different module to access (column 5, lines 54-67 to column 6, lines 1-17).

With regard to claim 4, Ku discloses the system, further including: a bus extension (Fig. 5, item 112), where at least one of the at least two modules is accessible via said bus extension (Fig. 5, item 622 and 622b); and where the transaction control is capable of providing to said bus extension an indication of said at least one of the modules, accessible via said bus extension, for access by the host processor; said transaction control is capable of providing to said bus extension an indication of said at

least one of the modules, accessible via said bus extension, for access by the embedded controller; and said bus extension is capable of providing an indication of said at least one of the modules for access by one of the processors (column 5, lines 2-61).

With regard to claims 5 and 6, Ku discloses the system, where the transaction control is capable of providing an indication of at least one of the at least two modules for access by one of the processors (column 5, lines 2-61), and where at least one of the at least two modules is part of an input/output chip (column 7, lines 20-59).

With regard to claim 53, Ku discloses a method for allowing an embedded controller (Fig. 5, item 620) to access at least two modules (Fig. 5, items 622 and 622b and Fig. 6, item 622) affiliated with a device, including the steps of: indicating the device (column 5, lines 54-61); indicating an access direction (read/write) (column 8, lines 61-65); indicating one of the at least two modules for accessing (column 5, lines 54-61); indicating a location for accessing, within said indicated one of the at least two modules (Fig. 6, item 622 and column 7, lines 20-59); and transferring data between said indicated location and the embedded controller (column 7, lines 41-50).

With regard to claims 54-55, Ku discloses the method where the indicated one of the at least two modules is accessible via a bus extension (Fig. 5, item 112), and where the step of indicating one of the at least two modules for accessing includes the step of:

indicating one of at least one chip select corresponding to said bus extension for accessing (column 5, lines 2-61).

With regard to claims 56-60, Ku discloses the method where indicated one of the at least two modules is part of an input/output chip (column 7, lines 20-59), and where the step of indicating a location for accessing includes the step of providing an indication of a location for accessing via an internal bus to said indicated one of said at least two modules, the method further including the step of: waiting for the freeing up of said internal bus before transferring said indication of a location for accessing onto said internal bus (column 5, lines 2-61).

Ku does not expressly disclose the system and method, where the system includes at least one access block bit controlled by one of the at least two processors for blocking access by another of the at least two processors to at least one of the at least two modules, as recited in claims 2, 50, and 53.

Glider discloses a system and method, where the system includes at least one access block bit controlled by one of the at least two processors for blocking access by another of the at least two processors to at least one of the at least two modules (column 5, lines 33-40).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Glider with Ku. The suggestion or motivation for doing so would have been to allow for real time sharing of resources without disrupting services provided by the system (column 1, lines 38-42).

Therefore, it would have been obvious to combine Glider with Ku to obtain the invention as specified in claims 2-6, 50-60, 72, and 73.

5. Claims 2-6, 50-60, and 70-73 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2002/0129184 to Watanabe in view of Glider.

With regard to claim 2, 3, 5, 72, and 73, Watanabe discloses a system (Fig. 1, item 100) for allowing shared access by at least two processors (Fig. 1, items 110 and 160) including an embedded controller (Figs. 1, 2A, and 2B, item 160) and a host processor (Figs. 1, 2A, and 2B, item 110) to at least two modules including (paragraph [0017]): at least two modules (Fig. 1, items 170 and 180); and a transaction control (Fig. 1, item 150); where the embedded controller is capable of providing an indication of which of the at least two modules to access to said transaction control; and the host processor is capable of providing an indication of which of the at least two modules to access to said transaction control (paragraph [0017]).

With regard to claims 4 and 6, Watanabe discloses the system, further including: a bus extension (Fig. 1, item 165), wherein at least one of the at least two modules is accessible via said bus extension; and wherein said transaction control is capable of providing to said bus extension an indication of said at least one of the modules, accessible via said bus extension, for access by the host processor; said transaction control is capable of providing to said bus extension an indication of said at least one of the modules, accessible via said bus extension, for access by the embedded controller; and said bus extension is capable of providing an indication of said at least one of the modules for access by one of the processors, and the system where at least one of the at least two modules is part of an input/output chip (paragraph [0015]).

With regard to claims 50-52, Watanabe discloses a method for allowing shared access to at least two modules by at least two processors including an embedded controller and a host processor (Figs. 1, 2A, and 2B), including the steps of: receiving an indication from each of the at least two processors of a module from among the at least two modules to access; arbitrating between the at least two processors in favor of one of the at least two processors; and accessing said module indicated by said one of the at least two processors (paragraphs [0017] and [0018]).

With regard to claim 53, Watanabe discloses a method for allowing an embedded controller to access at least two modules affiliated with a device (Fig. 2A), including the steps of: indicating the device (paragraphs [0017] and [0018]); indicating an access

direction (read/write) (paragraph [0015]); indicating one of the at least two modules for accessing (paragraphs [0017] and [0018]); indicating a location for accessing, within said indicated one of the at least two modules; and transferring data between said indicated location and the embedded controller (paragraphs [0017] and [0018]).

With regard to claims 54 and 55, Watanabe discloses the method where the indicated one of the at least two modules is accessible via a bus extension, and where the step of indicating one of the at least two modules for accessing includes the step of: indicating one of at least one chip select corresponding to said bus extension for accessing (Fig. 2A, item 170).

With regard to claims 56-60, Watanabe discloses the method where the indicated one of the at least two modules is part of an input/output chip (paragraph [0015]), where the step of indicating a location for accessing includes the step of providing an indication of a location for accessing via an internal bus to said indicated one of said at least two modules, the method further including the step of: waiting for the freeing up of said internal bus before transferring said indication of a location for accessing onto said internal bus (paragraphs [0018] and [0019]).

With regard to claims 70 and 71, Watanabe discloses the system and method, where at least one of the at least two modules includes a memory accessible through the bus extension (Fig. 1, item 180).

Watanabe does not expressly disclose the system and method, where the system includes at least one access block bit controlled by one of the at least two processors for blocking access by another of the at least two processors to at least one of the at least two modules, as recited in claims 2, 50, and 53.

Glider discloses a system and method, where the system includes at least one access block bit controlled by one of the at least two processors for blocking access by another of the at least two processors to at least one of the at least two modules (column 5, lines 33-40).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Glider with Watanabe. The suggestion or motivation for doing so would have been to allow for real time sharing of resources without disrupting services provided by the system (column 1, lines 38-42).

Therefore, it would have been obvious to combine Glider with Watanabe to obtain the invention as specified in claims 2-6, 50-60, and 70-73.

Response to Arguments

6. Applicant's arguments, see pages 11-14, filed July 9, 2004, with respect to the rejections of claims 2-6, 50-60, and 70-73 under 35 USC 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection are made in view of Lockwood and Glider.

The Examiner is persuaded that neither Ku nor Watanabe teach the system and method where at least one access block bit controlled by one of the at least two processors for blocking access by another of the at least two processors to at least one of the at least two modules, as recited in independent claims 2, 50, and 53. However, both Lockwood and Glider teach this feature.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (571) 272-3629. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKM

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